

Condensed Matter Physics Seminar Series

Can spintronics help make computing more efficient?

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In this talk, I discuss why computer designers are looking to develop novel ways of computing for a variety of common but specialized tasks, why spintronic devices, particularly magnetic tunnel junctions, might make valuable contributions to this process, and why success requires considering all levels of the computational stack from devices through the architecture. I illustrate these points in terms of three recent computational platforms my colleagues and I have worked on using magnetic tunnel junctions. The first example shows experimental results on binary neural networks based on crossbar arrays of magnetic tunnel junctions used as programmable resistors. Another describes using thermally unstable magnetic tunnel junctions to simulate associative memories. The final example is a simulation of a complex-valued Hopfield network using magnetic tunnel junctions as spin-torque oscillators.

Mark Stiles is a NIST Fellow in the Alternative Computing Group at the National Institute of Standards and Technology. He received a M.S./B.S. in Physics from Yale University, and a Ph.D. degree in Physics from Cornell University. Following postdoctoral research at AT&T Bell Laboratories, he joined the research staff at NIST. Mark's research has focused on the development of a variety of theoretical methods for predicting the properties of magnetic nanostructures and has recently shifted to studying alternative computing using novel hardware. He has helped organize numerous conferences, has served the American Physical Society on various committees, and has served on the editorial boards of several Physical Review journals. Mark is a Fellow of the American Physical Society and IEEE.

**Friday, February 28th at 10am
4-330 PAB**