UCLA Department of Physics & Astronomy

COLLOQUIUM

Thursday, June 5th at 4 p.m.
1-434 PAB

Hardware-efficient quantum error correction using concatenated bosonic qubits

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(Amazon AWS)

To solve problems of practical importance, quantum computers need error rates lower than 10^-10, whereas current quantum devices have error rates around 10^-3. To cover this gap, we will need to incorporate quantum error correction, where a logical qubit is redundantly encoded in many noisy physical qubits. Most often physical qubits are some energy levels of a physical element like an atom and are subject to both bit-flip and phase-flip errors. Alternatively, one can replace the physical qubit with qubit information redundantly encoded into a quantum harmonic oscillator (a bosonic qubit). In our experiment we use cat qubits, a type of bosonic qubit, where bit-flip errors are exponentially suppressed relative to phase-flip errors. The native bit-flip suppression means that an outer layer of quantum error correction only needs to focus on correcting the phase-flip errors. In the talk we will present our distance d=5 logical qubit memory made using a superconducting circuit. We will show that we can realize cat qubits with the exponential suppression of bit-flips and furthermore noise biased CNOT gates. We then discuss the performance of our logical memory formed from the concatenation of the encoded bosonic cat qubits with an outer repetition code of distance d=5. Throughout the talk we will remark on the interesting physical processes, such as engineered dissipation, that come together to realize our logical memory. Our work shows a path for realizing hardware-efficient quantum computing using bosonic qubits and biased noise.

Host: HongWen Jiang

Refreshments at 3:30 p.m. on the PAB Patio. Undergraduates Welcome!